ABSTRACT

[Abstract of the Disclosure]

Provided are a sigma-delta modulator and a fractional-N frequency synthesizer and including the fractional-N frequency synthesizer. The fractional-N frequency synthesizer includes a phase detector, a voltage controlled oscillator, a divider, and a sigma-delta modulator. The phase detector detects a phase difference between a reference signal and a feedback signal. The voltage controlled oscillator receives the phase difference signal detected by the phase detector and oscillates a signal with a desired frequency. The divider selects one from three or more integers according to a predetermined selection signal, divides the frequency of the signal output from the voltage controlled oscillator by the selected integer, and outputs a divided signal as the feedback signal to the phase detector. The sigma-delta modulator adds a predetermined input value to an internal feedback value, successively accumulates the added value, quantizes the finally accumulated value to three or more levels, and converts the quantization result into the predetermined selection signal.

[Representative Drawing]

FIG. 7

SPECIFICATION

[Title of the Invention]

SIGMA-DELTA MODULATOR AND FRACTIONAL-N FREQUENCY SYNTHESIZER COMPRISING THE SAME

[Brief Description of the Drawings]

FIG. 1 shows the configuration of a typical MASH $\Sigma-\Delta$ modulator;

FIG. 2 shows the configuration of a typical interpolative $\Sigma-\Delta$ modulator

FIG. 3 shows an input range and a mapping range of an output value of a single-bit 4^{th}-order $\Sigma-\Delta$ modulator;

FIG. 4 shows the relationship between a corner frequency of a quantization noise transfer curve and a pass band gain level;

FIG. 5A shows the quantization noise transfer curve of the single-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 3;

FIG. 5B shows the output of a PLL of the single-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 3;

FIG. 6 shows the result of autocorrelation for 2000 outputs of the single-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 3;

FIG. 7 is a block diagram of a fractional-N frequency synthesizer according to the present invention;

FIG. 8A is a block diagram of a 3-bit 4^{th}-order $\Sigma-\Delta$ modulator according to the present invention;

FIG. 8B is a detailed block diagram of a control signal generator shown in FIG. 8A;

FIG. 9 shows an input range and a mapped result of an output value of the 3-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 8A;

FIG. 10A shows a quantization noise transfer curve of the 3-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 8A;

FIG. 10B shows output phase noise of a PLL of the 3-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 8A; and

FIG. 11 shows an autocorrelation characteristic of the 3-bit 4^{th}-order $\Sigma-\Delta$ modulator shown in FIG. 8A.

[Detailed Description of the Invention]

[Object of the Invention]

[Technical Field of the Invention and Related Art prior to the Invention]

The present invention relates to a sigma-delta ($\Sigma-\Delta$) modulator and a fractional-N frequency synthesizer comprising the same, and more particularly, to a multi-bit multiple-order interpolative $\Sigma-\Delta$ modulator and a fractional-N phase-locked loop (PLL) frequency synthesizer comprising the same.

PLL frequency synthesizers synthesize desired signals using a reference signal and controls a ratio of the synthesized signal to the reference signal using a controller.

The PLL frequency synthesizers employ an integer-N technique and a fractional-N technique. The integer-N technique uses a fixed integer N in dividing an output frequency, and the fractional-N technique uses an integer N in dividing the output frequency which is selected among two or more integers. As a result, a divisor becomes fractional due to interpolation of each N selected at every dividing operation. As is known, the integer-N technique has a difficulty satisfying various specifications due to a trade-off between loop bandwidth and channel spacing, while the fractional-N technique alleviates design restrictions on PLLs owing to a broad loop bandwidth and narrow channel intervals.

The $\Sigma-\Delta$ modulator offers a control signal necessary for selecting N in the fractional-N technique.

The $\Sigma-\Delta$ modulator is classified into a MASH $\Sigma-\Delta$ modulator and an interpolative $\Sigma-\Delta$ modulator. As shown in FIG. 1, a first-order MASH $\Sigma-\Delta$

modulator forms an independent loop and is cascaded to another loop in order to construct a high-order modulator. Thus, the high-order modulator can be unconditionally stable and use most of an input range. However, the overall structure of the high-order modulator is complicated. The cascaded first-order modulator leads to a poor idle-tone characteristic. In order to improve the idle-tone characteristic, each node needs to remove the regularity of an output signal of the MASH $\Sigma-\Delta$ modulator through an independent dither that does not affect another node. When the MASH $\Sigma-\Delta$ modulator is a multi-bit modulator, a pass-band gain level of the multi-bit modulator is high, resulting in a large range of an output value change. Accordingly, in a fractional-N frequency synthesizer using the MASH $\Sigma-\Delta$ modulator, a non-linear error in a phase/frequency detector increases with the increase of the range of the output value change, which greatly limits the performance of the fractional-N frequency synthesizer.

The interpolative $\Sigma-\Delta$ modulator has a structure as shown in FIG. 2. The structure of the interpolative $\Sigma-\Delta$ modulator is far more simplified than the MASH $\Sigma-\Delta$ modulator. In addition, when the interpolative $\Sigma-\Delta$ modulator is used as a multi-bit modulator, the interpolative $\Sigma-\Delta$ modulator has a lower pass-band gain level than the MASH $\Sigma-\Delta$ modulator, resulting in a small range of an output value change.

In consideration of the above characteristics, Sang-Oh Lee et al. presented a fractional-N frequency synthesizer using a single-bit 4^{th}-order $\Sigma-\Delta$ modulator ("A 17mW, 2.5GHz Fractional-N Frequency Synthesizer for CDMA-2000", IEEE ESSCIRC, pp. 40-43, September 18, 2001). The single-bit 4^{th}-order $\Sigma-\Delta$ modulator shows a relatively good performance but has a few problems. First, the single-bit 4^{th}-order $\Sigma-\Delta$ modulator is not as unconditionally stable as the MASH $\Sigma-\Delta$ modulator and thus uses only a limited input range for guaranteeing stability. In other words, a dead band takes place in the full input range. In order to solve this problem, as shown in FIG. 3, the single-bit 4^{th}-order $\Sigma-\Delta$ modulator uses only 50% of the full input range and maps an output value into N-1 or N+1. This results in 1 bit loss and an increase in quantization noise by 6dB.

In addition, a quantization noise transfer function of the single-bit 4th-order $\Sigma-\Delta$ modulator shows the characteristic of a high-pass filter. When the single-bit 4th-order $\Sigma-\Delta$ modulator is of an interpolative type, a pass band gain level needs to be less than a threshold in order to maintain stability. The pass band gain level is generally adjusted using a Butterworth filter coefficient. Since a total amount of the quantization noise is maintained to be constant, the threshold and a corner frequency of the pass band gain level show a trade-off tendency as seen in FIG. 4. In other words, the pass band gain level increases when the corner frequency increases, and the pass band gain level decreases when the corner frequency decreases.

When f_s is an operation frequency, the maximum corner frequency that guarantees the stability of the single-bit 4th-order $\Sigma-\Delta$ modulator is $0.06*f_s$. FIGS. 5A and 5B respectively show a quantization noise transfer curve of the single-bit 4th-order $\Sigma-\Delta$ modulator and the output of a PLL with respect to frequency. In FIG. 5B, slanted line 60 denotes out-of-band phase noise of a voltage controlled oscillator (VCO) of the PLL. As can be seen in FIG. 5B, phase noise of the PLL becomes greatly worse near the corner frequency of the single-bit 4th-order $\Sigma-\Delta$ modulator.

Lastly, the single-bit 4th-order $\Sigma-\Delta$ modulator without dithering always has an idle-tone problem. FIG. 6 shows the result of autocorrelation for 2000 outputs of the single-bit 4th-order $\Sigma-\Delta$ modulator. As can be seen in FIG. 6, the autocorrelation result varies within a large range.

Accordingly, a $\Sigma-\Delta$ modulator and a stable fractional-N frequency synthesizer using the $\Sigma-\Delta$ modulator are required to solve the above problems.

[Technical Goal of the Invention]

The present invention provides a multi-bit multiple-order interpolative sigma-delta ($\Sigma-\Delta$) modulator that has no burden of increase of hardware in comparison with a single-bit $\Sigma-\Delta$ modulator by minimizing the hardware through metallic connection and a fractional-N frequency synthesizer using the multi-bit multiple-order interpolative $\Sigma-\Delta$ modulator.

[Structure and Operation of the Invention]

According to an aspect of the present invention, there is provided a fractional-N frequency synthesizer including a phase detector, a voltage controlled oscillator, a divider, and a sigma-delta modulator. The phase detector detects a phase difference between a reference signal and a feedback signal. The voltage controlled oscillator receives the phase difference signal detected by the phase detector and oscillates a signal with a desired frequency. The divider selects one from three or more integers according to a predetermined selection signal, divides the frequency of the signal output from the voltage controlled oscillator by the selected integer, and outputs a divided signal as the feedback signal to the phase detector. The sigma-delta modulator adds a predetermined input value to an internal feedback value, successively accumulates the added value, quantizes the finally accumulated value to three or more levels, and converts the quantization result into the predetermined selection signal.

According to another aspect of the present invention, there is provided a sigma-delta modulator including a plurality of operation units, a quantizer, and a plurality of multipliers. The plurality of operation units add input values to internal feedback values and sequentially accumulates the added values up to a 4^{th}-order. The quantizer quantizes a value output from the last one of the logic units into multi-bits. The plurality of multipliers output feedback coefficients determined in correspondence with a plurality of levels quantized by the quantizer as the feedback values to the operation units.

Hereinafter, embodiments of the present invention will be described in detail with reference to the attached drawings.

FIG. 7 is a block diagram of a fractional-N frequency synthesizer according to the present invention. Referring to FIG. 7, the fractional-N frequency synthesizer has a feedback loop which divides an output signal f_{out} of the fractional-N frequency synthesizer and then outputs a phase control signal f_d. The division of the output signal f_{out} is achieved by a divider 13 and a $\Sigma-\Delta$ modulator 14 which controls a division ratio of the divider 13. The divider 13 divides the output signal f_{out} using a

value that is selected from two or more integers according to a selection signal output from the $\Sigma-\Delta$ modulator 14. It is preferable that the $\Sigma-\Delta$ modulator 14 is a multi-bit multiple-order $\Sigma-\Delta$ modulator, which will be described later. Here, in the present embodiment, a 3-bit 4th-order $\Sigma-\Delta$ modulator will be explained. The phase control signal f_d is input to a phase detector (PD) 10 and then compared with a reference signal f_{ref}. The PD 10 outputs a control signal with a direct current voltage proportional to a phase difference between the phase control signal f_d and the reference signal f_{ref}. The control signal passes through a low-pass filter (LPF) 11 and then is input to a VCO 12. The VCO 12 then outputs the output frequency f_{out} according to the input control signal.

FIG. 8A is a block diagram of the 3-bit 4th-order $\Sigma-\Delta$ modulator. Referring to FIG. 8A, the 3-bit 4th-order $\Sigma-\Delta$ modulator includes a first operation unit 80, a second operation unit 81, a third operation unit 82, a fourth operation unit 83, a 3-bit quantizer 84, and a control signal generator 85. The first operation unit 80 includes a feedback coefficient multiplier 801, an adder 802, an accumulator (ACC) 803, and a dynamic scaling coefficient multiplier 804. The ACC 803 may include an adder (not shown) and a delayer (not shown) which are interconnected.

The operation of the 3-bit 4th-order $\Sigma-\Delta$ modulator will now be explained. The first, second, third, and fourth operation units 80, 81, 82, and 83 perform in a similar way. Thus, only the behavior of the first operation unit 80 will now be described herein. The feedback coefficient multiplier 801 determines one among 8 feedback coefficients by combining control signals generated from outputs of the 3-bit 4th-order $\Sigma-\Delta$ modulator and then outputs the determined feedback coefficient to the adder 802. The adder 802 adds the determined feedback coefficient to a frequency control value input within an input range. The ACC 803 accumulates a value output from the adder 802, and the dynamic scaling coefficient multiplier 804 multiplies the accumulated value by a dynamic scaling coefficient. The addition and accumulation are performed to the fourth operation unit 83. Thereafter, the 3-bit quantizer 84 quantizes a value output from the fourth operation unit 83 to 8 level one. The quantized value is output to the divider 13

and then output as a selection signal for selecting one from 8 output values ranging from N-3 to N+4. If a 2- or 4- bit quantizer is used, the divider 13 selects 4 or 16 values, i.e., one from 2^n values, where n is 2 or 4.

When the quantized value is also input to the control signal generator 85, the control signal generator 85 generates control signals to provide the feedback coefficient multipliers 801, 811, 821, and 831 of the first, second, third, and fourth operation units 80, 81, 82, and 83.

The 3-bit 4th-order $\Sigma-\Delta$ modulator can solve the problems incurred in the prior art. In other words, an output level increases to 8 levels which are mapped from N-3 to N+4 as shown in FIG. 9. Thus, although only 1/8 of the full input range is used, the output level can be mapped to N or N+1. In addition, quantization noise is attenuated, which leads a corner frequency to be higher. Compared to single-bit quantization, 3-bit quantization reduces quantization noise to 1/8. FIG. 10A shows a quantization noise transfer curve of the 3-bit 4th-order $\Sigma-\Delta$ modulator shown in FIG. 8A. As can be seen in FIG. 10A, the corner frequency of the 3-bit 4th-order $\Sigma-\Delta$ modulator is increased by double or more from of the single-bit 4th-order $\Sigma-\Delta$ modulator shown in FIG. 5A. FIG. 10B shows output phase noise of a PLL of the 3-bit 4th-order $\Sigma-\Delta$ modulator shown in FIG. 8A. Unlike in the single-bit 4th-order $\Sigma-\Delta$ modulator, phase noise of the PLL of the 3-bit 4th-order $\Sigma-\Delta$ modulator does not surpass a slanted line 60, which results in improvement of out-of-band phase noise.

Also, the three-bit 4th-order $\Sigma-\Delta$ modulator shows a good idle-tone characteristic as shown in FIG. 11. FIG. 11 shows the result of autocorrelation for 2000 output samples of the 3-bit 4th-order $\Sigma-\Delta$ modulator. The output range of autocorrelation of the forgoing 2000 output samples is reduced to about 1/10 of that of FIG. 6.

It is most burdensome to implement the feedback coefficient multipliers 801, 811, and 821, and 831, and the dynamic scaling coefficient multipliers 804, 814, and 824 in constructing the 3-bit 4th-order $\Sigma-\Delta$ modulator as hardware. Since scaling coefficients can be generally realized in the form of the square of 2, the dynamic scaling

coefficient multipliers 804, 814, and 824 can be realized by a simple shift operation. However, feedback coefficients may require the critical increase of hardware. Therefore, considering a direct implementation of the feedback coefficients in hardware without the use of the feedback coefficient multipliers 801, 811, 821, and 831, it may be an answer that the feedback coefficients are stored in a read-only memory (ROM) in advance. Whenever necessary, corresponding feedback coefficients can be read from the ROM to be output to the adder 802, 812, 822, and 832 of the operation units 80, 81, 82, and 83, respectively. However, in a case of 3-bit output, it is greatly burdensome to select one coefficient from 8 coefficients. In addition, since the feedback values are input to each of the logic units 80, 81, 82, and 83, four paths are formed in the present invention. Accordingly, a ROM medium to store 32 coefficients is required, and a total capacity of 640 bits of ROM is required even though a 20-bit register is used for one coefficient. Thus, a method of realizing multipliers through only metallic connections is taken into account to reduce the burden to the realization of hardware.

Table 1 below shows outputs of the 3-bit quantizer 84, expressed as normalized feedback coefficients at equal intervals in order to realize the multipliers through only the metallic connection.

[Table 1]

coefficient 1	0.875
coefficient 2	0.625
coefficient 3	0.375
coefficient 4	0.125
coefficient 5	-0.125
coefficient 6	-0.375
coefficient 7	-0.625
coefficient 8	-0.875

Table 2 below shows 20-bit feedback coefficient example which is actually provided to each operation unit in the above pattern.

[Table 2]

Bit Group	20		19	18	17	16	15								5	4	3	2	1
Coefficient 1	0		0	1	0	1	0		·	·	·	·	·		0	1	0	0	0
Coefficient 2	0		0	0	1	1	1		·	·	·	·	·		0	1	0	0	0
Coefficient 3	0		0	0	1	0	0		·	·	·	·	·		1	1	0	0	0
Coefficient 4	0		0	0	0	0	1		·	·	·	·	·		1	1	0	0	0
Coefficient 5	1		1	1	1	1	0		·	·	·	·	·		0	1	0	0	0
Coefficient 6	1		1	1	0	1	1		·	·	·	·	·		0	1	0	0	0
Coefficient 7	1		1	1	0	0	0		·	·	·	·	·		1	1	0	0	0
Coefficient 8	1		1	0	1	0	1		·	·	·	·	·		1	1	0	0	0

In Table 2, since one feedback coefficient is expressed with 20 bits, 2^{20} bit combinations are possible. However, each bit group, which represents 8 feedback coefficients at the same time, is expressed with 8 bits and thus has a number of 2^8 available bit combinations. The present invention adopts a way to simultaneously express 8 feedback coefficients in each operation unit through combinations of bit groups and minimizes a number of combinable signals of bit groups for hardware minimization.

As can be seen in Table 2, first through fourth bit groups each contain coefficients 1 through 8 with equal bit values, and fifth through twelfth bit groups each contain coefficients 1 through 8, in which coefficients 5 through 8 have inverted bit values with respect to bit values of coefficients 4 through 1. The inversion of bit values is due to the expression of feedback coefficients through the conversion of a value output from the 3-bit quantizer 84 into a symmetrical gray code signal. Here, a number of signals of available bit groups is 2^4 according to the symmetrical characteristic.

When the above characteristic is realized into hardware, for bit groups with equal bit values, the values of "0" or "1" are connected directly to the adder 802, 812, and 822. For bit groups with inverted bit values, control signals generated from outputs of the

3-bit quantizer 84 so as to show the inversion characteristic as shown in Table 2 are input directly to the adder 802, 812, and 822, respectively, through metallic connections.

When describing the bit groups with inverted bit values, a total of 16 generable controls signals, of which 8 control signals are inverted with respect to the remaining 8 control signals. Thus, in a case where the control signal generator 8 converts a value output from the 3-bit quantizer 84 into gray code data to make 8 control signals, the feedback coefficient multipliers 801, 811, 821, and 831 can be realized only through metallic connections along with 8 control signals with hardly increasing hardware. In the present embodiment, since the 3-bit quantizer 84 is used, 8 control signals are necessary. However, when a 2-bit quantizer is used, 2 control signals are required. When a 4-bit quantizer is used, 128 control signals are needed.

FIG. 8B is a detailed block diagram of the control signal generator 85. Referring to FIG. 8B, the control signal generator 85 includes a gray coder 850, a plurality of control signal generating unit 851, and a plurality of inverters 852.

The gray coder 850 converts the output from the 3-bit quantizer 84 into the gray code data. Since the control signal generating units 851 include a variety of logic units such as AND gates and the like, they receive the gray code data, output a portion of the results as shown in Table 2 via the inverters 852. Accordingly, the control signal generator 85 can generate 8 control signals from a 3-bit output of the 3-bit quantizer 84. In addition, the control signal generator 85 can contribute to the realization of the feedback coefficient multipliers 801, 811, 821, and 831, and the dynamic scaling coefficient multipliers 804, 814, and 824 through only metallic connections by combining 8 control signals and inverted signals according to Table 2.

[Effect of the Invention]

As described above, in the present invention, a single-bit modulator can be configured into a single multi-bit modulator. The multi-bit modulator enables a usable input range to be reduced and an output level to be increased compared to the single-bit modulator. As a result, only 1/8 of the full input range of the multi-bit

modulator can be mapped into N or N+1. In addition, the multi-bit modulator can reduce quantization noise and thus allow a corner frequency to be higher. Moreover, an increase in hardware can be minimized by realizing multipliers through only metallic connections.

5

What is claimed is:

1. A fractional-N frequency synthesizer comprising:

a phase detector that detects a phase difference between a reference signal and a feedback signal;

a voltage controlled oscillator that receives the phase difference signal detected by the phase detector and oscillates a signal with a desired frequency;

a divider that selects one from three or more integers according to a predetermined selection signal, divides the frequency of the signal output from the voltage controlled oscillator by the selected integer, and outputs a divided signal as the feedback signal to the phase detector; and

a sigma-delta modulator that adds a predetermined input value to an internal feedback value, successively accumulates the added value, quantizes the finally accumulated value to three or more levels, and converts the quantization result into the predetermined selection signal.

2. The fractional-N frequency synthesizer of claim 1, wherein the sigma-delta modulator comprises:

a plurality of operation units that adds the predetermined input value to the internal feedback value and successively accumulates the added value a plurality of times;

a quantizer that quantizes a value output from the last one of the plurality of operation units to multi-bits and outputs the quantized value as the selection signal to the divider; and

a plurality of multipliers that output feedback coefficients determined in correspondence with a plurality of levels quantized by the quantizer as the feedback values to the operation units, respectively.

3. The fractional-N frequency synthesizer of claim 2, wherein the feedback coefficients are symmetrical values at equal intervals around a middle level of the plurality of levels output from the quantizer.

4. The fractional-N frequency synthesizer of claim 3, wherein the feedback coefficients are converted into bit streams with binary values so as to be suitable for implementing hardware.

5. The fractional-N frequency synthesizer of claim 4, wherein the multipliers further comprise a control signal generator that receives a plurality of bit values output from the quantizer and outputs the minimum number of control signals depending on the symmetrical characteristic of the bit streams.

6. The fractional-N frequency synthesizer of claim 5, wherein the control signal generator comprises:

a gray coder that converts the plurality of bit values into a gray code;

a plurality of control signal generating units that receive the gray code and output the control signals;

a plurality of inverters that invert outputs of the control signal generating units, respectively.

7. The fractional-N frequency synthesizer of any one of claims 5 and 6, wherein the multipliers comprise metal connections through which the bit streams are output from the control signals output from the control signal generator directly to the corresponding operation units.

8. A sigma-delta modulator comprising:

a plurality of operation units that add input values to internal feedback values and sequentially accumulates the added values up to a 4^{th}-order;

a quantizer that quantizes a value output from the last one of the logic units into multi-bits; and

a plurality of multipliers that output feedback coefficients determined in correspondence with a plurality of levels quantized by the quantizer as the feedback values to the operation units.

9. The sigma-delta modulator of claim 8, wherein the feedback coefficients are symmetrical values at equal intervals around a middle level of the plurality of levels output from the quantizer.

10. The sigma-delta modulator of claim 9, wherein the feedback coefficients are converted into bit streams with binary values so as to be suitable for implementing hardware.

11. The sigma-delta modulator of claim 10, wherein the multipliers further comprise a control signal generator that receives a plurality of bit values output from the quantizer and outputs the minimum number of control signals depending on the symmetrical characteristic of the bit streams.

12. The sigma-delta modulator of claim 11, wherein the control signal generator comprises:

a gray coder that converts the plurality of bit values into a gray code;

a plurality of control signal generating units that receive the gray code and output the control signals;

a plurality of inverters that invert outputs of the control signal generating units, respectively.

13. The sigma-delta modulator of any one of claims 11 and 12, wherein the multipliers comprise metal connections through which the bit streams are output from

the control signals output from the control signal generator directly to the corresponding operation units.

FIG. 1 (PRIOR ART)

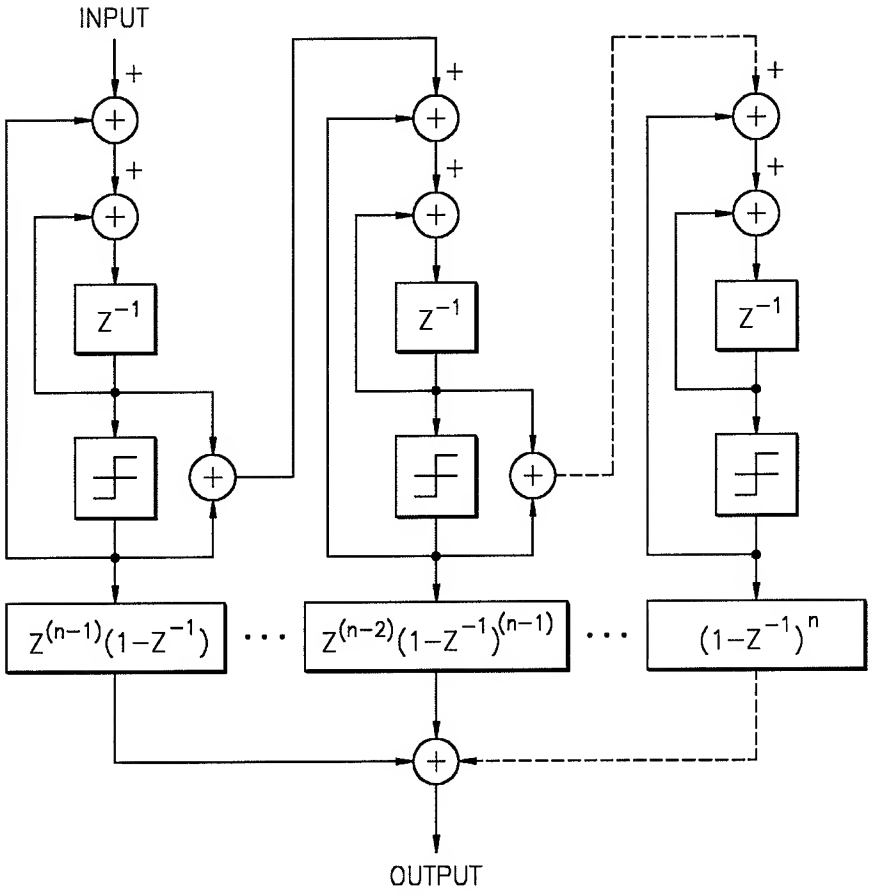


FIG. 2 (PRIOR ART)

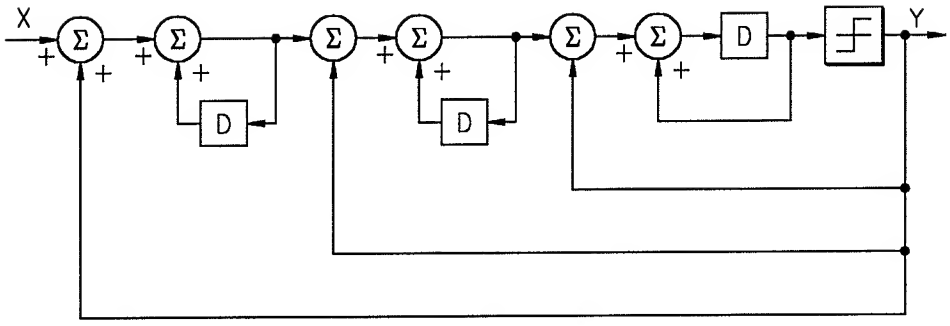


FIG. 3

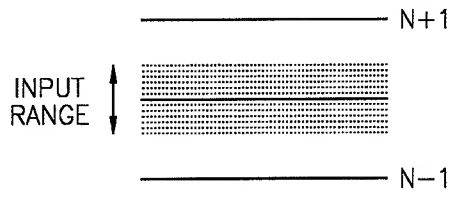


FIG. 4 (PRIOR ART)

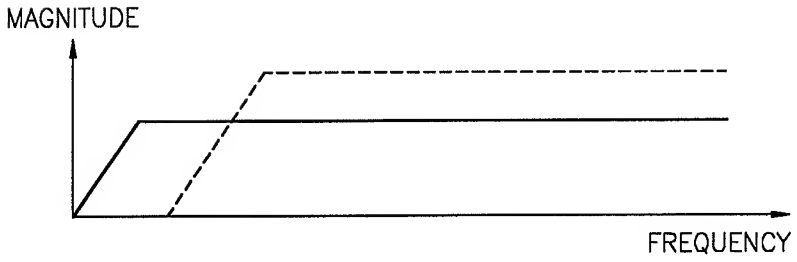


FIG. 5A (PRIOR ART)

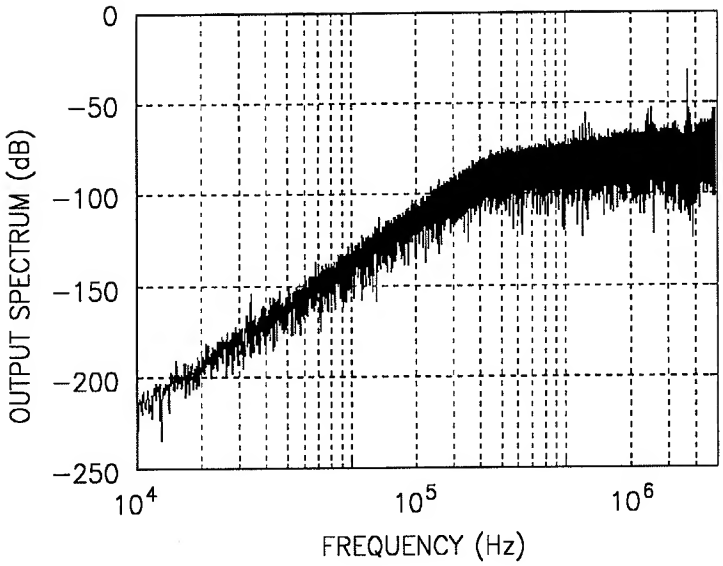


FIG. 5B (PRIOR ART)

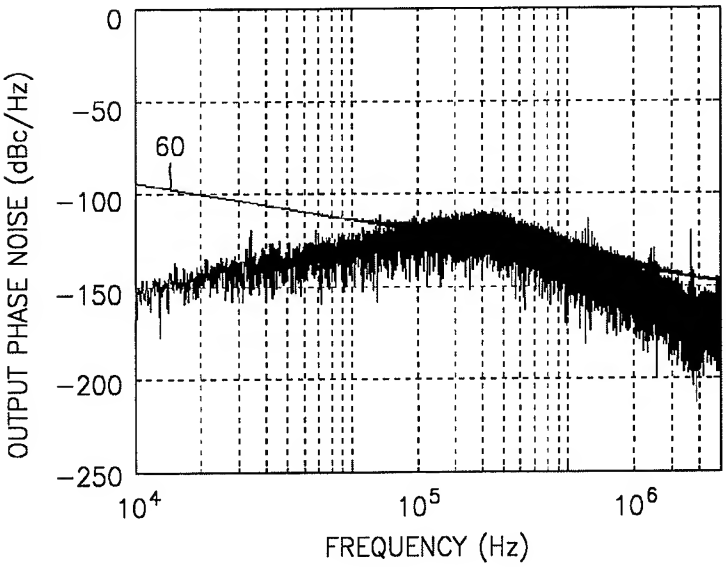


FIG. 6 (PRIOR ART)

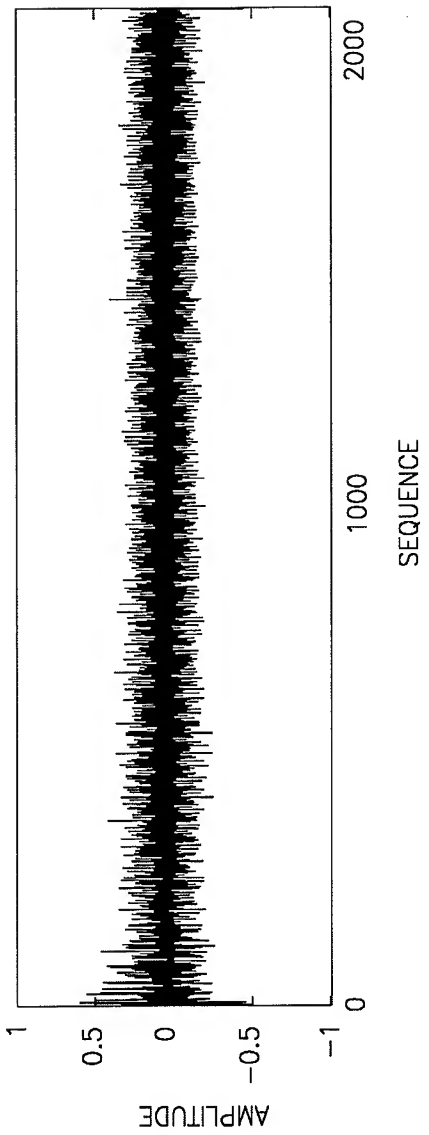


FIG. 7

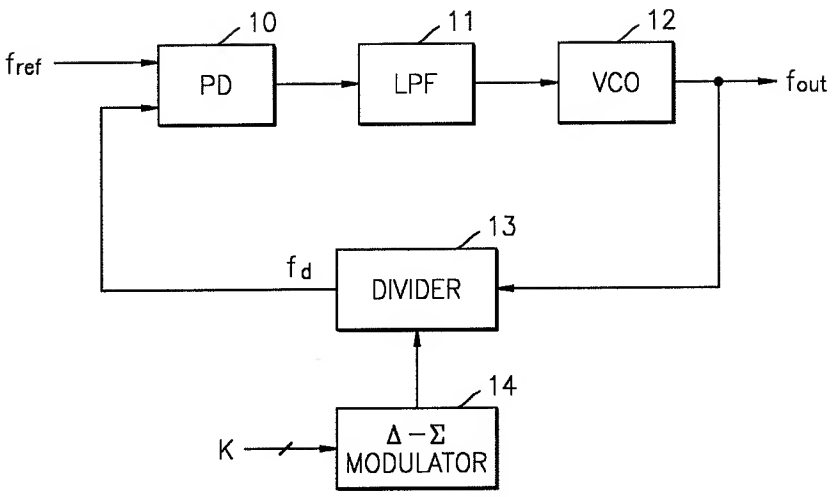


FIG. 8A

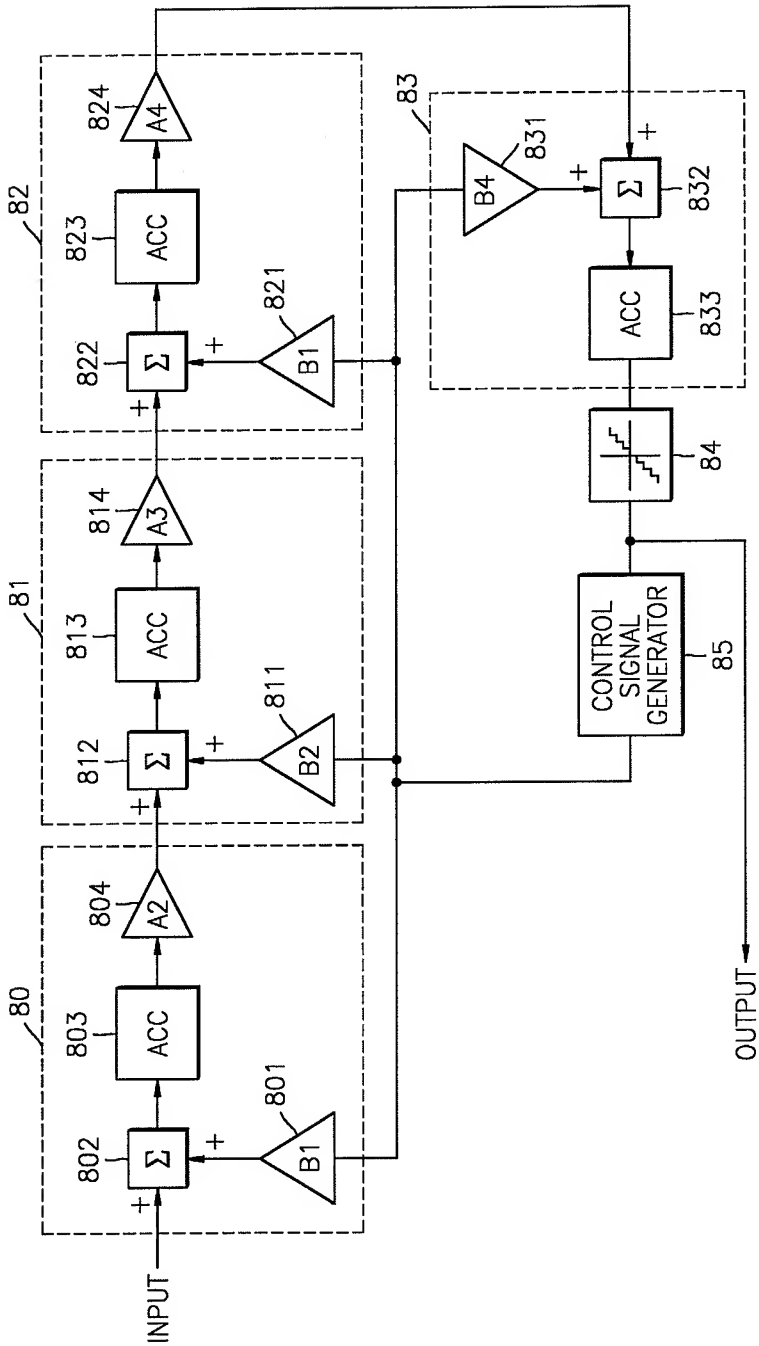

INPUT
80
802
Σ
801
B1
803
ACC
804
A2
81
812
Σ
811
B2
813
ACC
814
A3
82
822
Σ
821
B1
823
ACC
824
A4
83
B4
831
Σ
832
ACC
833
84
CONTROL SIGNAL GENERATOR
85
OUTPUT

FIG. 8B

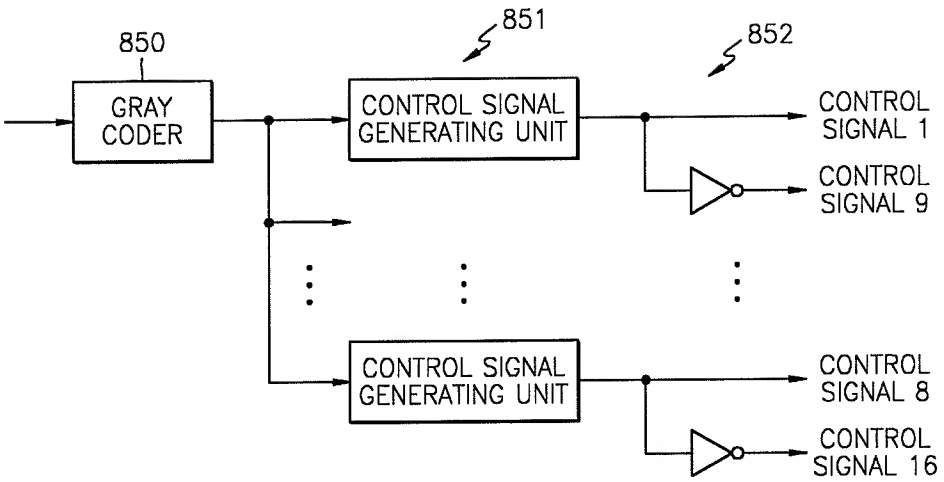

850
851
852
GRAY CODER
CONTROL SIGNAL GENERATING UNIT
CONTROL SIGNAL GENERATING UNIT
CONTROL SIGNAL 1
CONTROL SIGNAL 9
CONTROL SIGNAL 8
CONTROL SIGNAL 16

FIG. 9

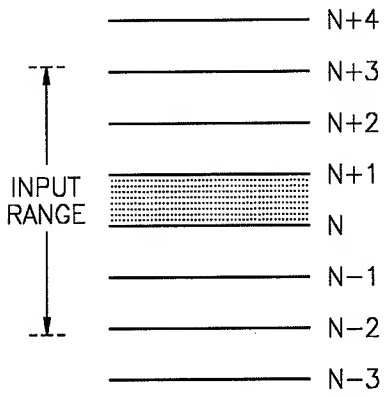

N+4
N+3
N+2
N+1
N
N−1
N−2
N−3
INPUT RANGE

FIG. 10A

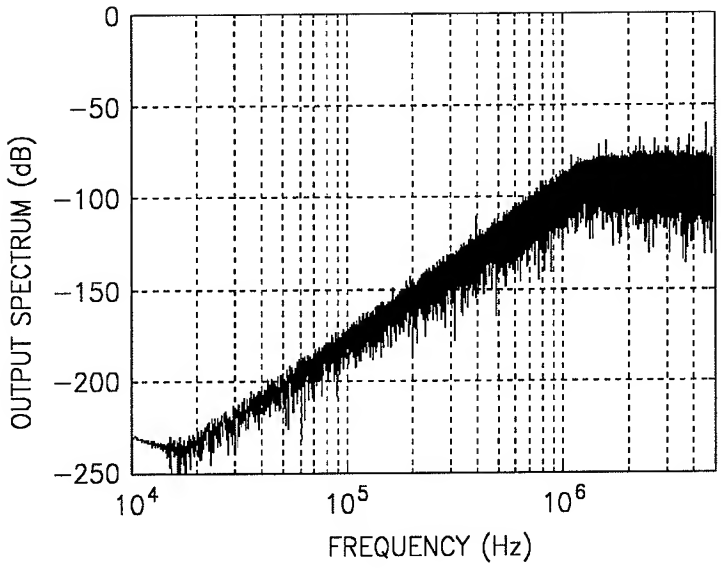


FIG. 10B

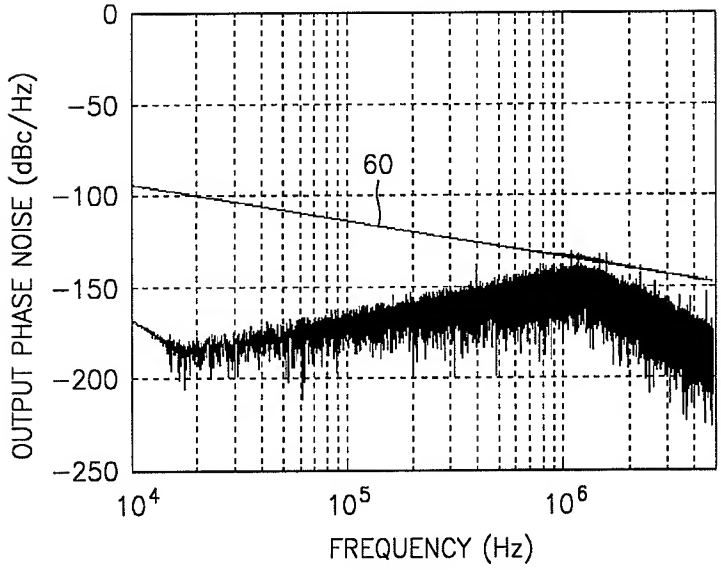
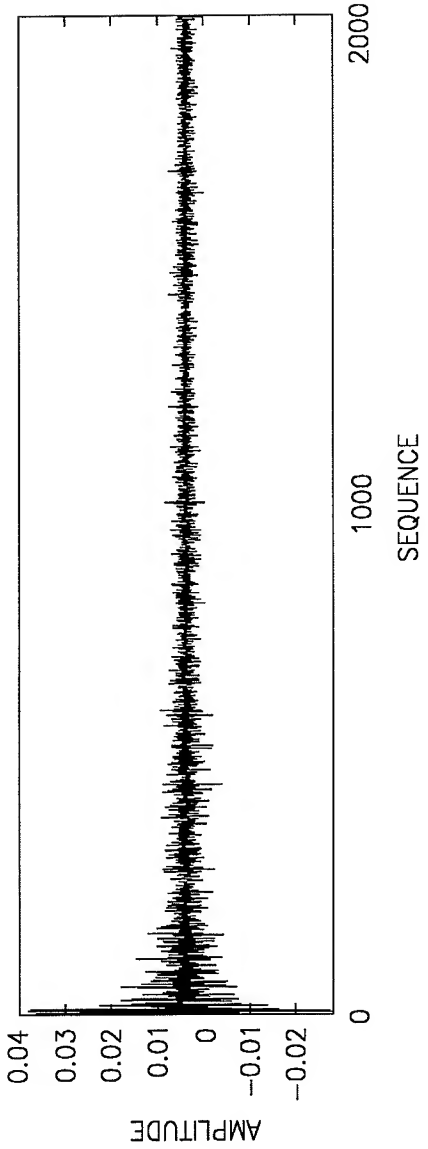


FIG. 11



CERTIFICATION OF TRANSLATION

I, ***Seung-hye Kim***, an employee of Y.P.LEE, MOCK & PARTNERS of Koryo Bldg., 1575-1 Seocho-dong, Seocho-gu, Seoul, Republic of Korea, hereby declare under penalty of perjury that I understand the Korean language and the English language; that I am fully capable of translating from Korean to English and vice versa; and that, to the best of my knowledge and belief, the statement in the English language in the attached translation of ***Korean Patent Application No. 10-2002-0073050*** consisting of ***25*** pages, have the same meanings as the statements in the Korean language in the original document, a copy of which I have examined.

Signed this 20th day of February 2008